www.FirstRanker.com www.FirstRank

Code: R7420406

1

IV B.Tech II Semester(R07) Regular Examinations, April 2011 DSP PROCESSORS & ARCHITECTURES

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE questions All questions carry equal marks

1. For the FIR filter

$$Y(n) = [x(n) + x(n-1) + x(n-2)]/3$$

Determine the:

- (a) System function
- (b) Magnitude response function
- (c) Phase response function
- (d) Impulse response
- (e) Step response
- (f) Poles and zeros.
- 2. (a) Compute the dynamic range and percentage resolution of a signal that uses.
 - i. 16-point fixed-point format.
 - ii. 32-point floating-point format with 24 bits for the mantissa and 8 bits for the exponent.
 - (b) Write the brief notes on A/D conversion errors.
- 3. (a) Draw a structure of 8X8 Braun multiplier.
 - (b) Draw the neat diagram of MAC with accumulator guard bit and explain in detail.
- 4. (a) Explain when a program can make all the four functional units in the CPU to do productive work in all the cycles.
 - (b) Draw the table showing the content of the instruction pipeline when each of the following program is executed. Program is: LAR AR1#167h.

LACC#164h

SAMM AR2

NOP

LACC *+

ADD *+

SACL*+

LAMM AR2.

- 5. (a) Explain The difference between the internal and external modes of clocking TMS 320C54XX processors how do you vary the clock frequency in each case?
 - (b) Write a TMS 320C54XX program to mask the lower 6 bits of a word stored in the data memory and write the modified word back at the same location.
- 6. (a) Determine the value of each of the following 16-bit numbers represented using the given Q-notation:
 - i. 4400h as a Q0 number
 - ii. 4400h as a Q15 number
 - iii. 4400h as a Q7 number
 - iv. 3400h as a Q0 number.
 - (b) Write a brief notes on interpolation filter with suitable example.
- 7. (a) Implement the 8-point DIFFFT butterfly.
 - (b) Write a subroutine to compute the signal spectrum using result of 8-point FFT on TMS320c54XX.
- 8. (a) Explain clearly how does DMA help in increasing the processing speed of a DSP processor?
 - (b) How does the interrupt handling in the TMS320c54XX DSP differ for a software and hardware interrupt.

www.FirstRanker.com www.FirstRank

Code: R7420406

IV B.Tech II Semester(R07) Regular Examinations, April 2011 DSP PROCESSORS & ARCHITECTURES

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering) Time: 3 hours Max Marks: 80

Answer any FIVE questions All questions carry equal marks

1. For IIR filter
$$H(z) = \frac{(z-1)}{(z-.025)(z-0.5)}$$
 Determine the

Determine the:

- (a) magnitude response function
- (b) Phase response function
- (c) Impulse response
- (d) Step response
- (e) Poles and zeros
- (a) Write a brief note on following:
 - i. DSP computational errors
 - ii. D/A conversion errors.
 - (b) Show that the dynamic range of a signal increases by 6db for each additional bit used to represent
- (a) How will you implement an 8X8 multiplier using 4X4 multipliers as the building blocks?
 - (b) What distinguishes a digital signal processor from a general-purpose micro-processor with regard to basic capabilities?
- (a) Draw the table showing the content of the instruction pipeline when each of the following program is executed.

LDP 20hProgram is: LACC 30hSub #30hBCND YY,GTВ YYXXNEG YYSACL 30h

- (b) Explain when a program can make all the four functional units in the CPU to do productive work in all the cycles.
- 5. With suitable diagrams explain the internal and external modes of clocking TMS320C54XX processors. How do you vary the clock frequency in each case?
- (a) Write a brief notes on decimation filters with suitable example?
 - (b) Write short notes on adaptive filters.
- 7. (a) Draw the signal flow graph for an 8-point DFT computation and explain implementations.
 - (b) Write a subroutine to compute the signal spectrum using the result of the 8-point FFT on TMS320C54XX.
- (a) What are the various classifications of interrupts for the TMS320C5416 processor?
 - (b) With neat diagram explain the CODEC interface circuit.

www.FirstRanker.com www.FirstRank

Code : R7420406

3

IV B.Tech II Semester(R07) Regular Examinations, April 2011 DSP PROCESSORS & ARCHITECTURES

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE questions All questions carry equal marks

1. (a) Given the sequences.

$$x_1(n) = \begin{bmatrix} 3 & 4.2 & 11 & 0 & 7 & -1 & 0.2 \end{bmatrix}$$

 $x_2(n) = \begin{bmatrix} 1.2 & 3 & 0 & -0.52 \end{bmatrix}$

Compute and plot the sequence $x_1(n) * x_2(n)$. Determine the length of the computed sequence.

- (b) Write the MAT LAB program for 11R filter.
- 2. (a) Compute the dynamic range and the percentage resolution for a block floating-point format with a 4 bit exponent used in a 16-bit fixed-point processor.
 - (b) Write the brief note on:
 - i. Compensating filters.
 - ii. DSP computational errors.
- 3. (a) What distinguishes a digital signal processor from a general-purpose micro-processor with regard to basic capabilities?
 - (b) Draw the structure of a 8X8 Braun multiplier.
- 4. (a) Explain how pipeline conflicts occurs when the program memory and data memory space of a program are contained in external memory space.
 - (b) Draw the table showing the content of the instruction pipeline when each of the following program are executed.

Program is:

LAR ARI,#167h.

LACC #164h

SAMM AR2

LACC *+

ADD *+

SACL *+

LAMM AR2

- 5. Identify the addressing mode of the source operand in each of the following instructions:
 - (a) ADD *AR2,A
 - (b) ADD *AR2+,A
 - (c) ADD *AR2+%,A
 - (d) ADD #offh, A
 - (e) ADD 1234h,A
 - (f) ADD *AR2+OB,A
 - (g) ADD *+AR2,A
 - (h) ADD +*AR2,A.
- 6. (a) Represent each of the following as 16-bit numbers in the desired Q-notation.
 - i. 0.3125 as a Q15 number.
 - ii. -0.3125 as a Q15 number.
 - iii. 3.125 as a Q7 number.
 - iv. -352 as a Q0 number.
 - (b) Write notes on 2-D signal processing.
- 7. Derive the optimum scaling factor for the DIF FFT butterfly.
- 8. (a) Draw & explain the flow chart of interrupt handling by the TMS320C54XX.
 - (b) With suitable timing diagrams explain I/O interface signals for read-write operation.

www.FirstRanker.com www.FirstRank

Code: R7420406



IV B.Tech II Semester (R07) Regular Examinations, April 2011 DSP PROCESSORS & ARCHITECTURES

(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE questions All questions carry equal marks

- 1. (a) Write MAT LAB programs for FIR filter.
 - (b) Assuming X(k) as a complex sequence, determine the number of complex and real multiplies for computing IDFT using direct and radix-2 FFT algorithms.
- 2. (a) Show that the dynamic range of a signal increases by 6dB for each additional bit used to represent its value.
 - (b) Compute the dynamic range and the percentage resolution for a block floating-point format with a 4-bit exponent used in a 16 bit fixed-point processor.
- 3. (a) How will you implement an 8X8 multiplier using 4X4 multipliers as the building blocks?
 - (b) Explain about MAC unit, draw the diagram of MAC unit.
- 4. (a) Draw the table showing the content of the instruction pipeline when each of program is executed.

rogram is :	LAR AR1,	1200h
	LAR AR2,	1300h
	LAR AR3,	02h
	MAR^* ,	AR1
XX	LACC*+,	AR2
	SACC*+,	AR3
	BANZ XX,	AR1
	ADD*-	
	ADD*-	

(b) Explain when a program can make all the four functional units in the CPU to do productive work in all the cycles.

NXCI

- 5. (a) Write a sequence of TMS320C54XX instructions to configure a circulars buffer with a start address at 0200h and an end address at 021FH with current buffer pointer (AR6) pointing to address 0205h.
 - (b) Write a TMS320C54XX program to compute the equation. Y=mx+C Assume that 'x' and 'C' are stored in the data memory and 'm' in the program memory. The result should be stored in the data memory.
- 6. (a) Determine the linearly interpolated sequence from the given sequence.

 $x(n) = \begin{bmatrix} 0 & 4 & 8 & 12 & 16 & 12 & 84 & 0 \end{bmatrix}$

For an interpolation factor of 3 what interpolating sequence h(n) can achieve the specified interpolation?

- (b) Explain with an example how PID controller is implemented using TMS320C54XX.
- 7. (a) Write about scaling and overflow in FFT algorithms?
 - (b) What minimum size FFT must be used to compute a DFT of 40 points? What must done to the samples before the chosen FFT is applied?
- 8. (a) What are the various classifications of interrupts for the TMS320C5416 processor?
 - (b) Explain CODEC DSP interfacing with an example.
